METHOD AND CIRCUIT FOR DE-SKEWING DATA IN A COMMUNICATION SYSTEM

ABSTRACT OF THE DISCLOSURE

Method and circuitry for de-skewing data in data communication networks such as a SONET. The data is sent from a system chip to a framer chip where the data is de-skewed. To detect data skew, the system chip sends a training sequence to the framer chip. The information bits sent to the framer chip are searched in order to detect the training sequence. The training sequences contain clear transition patterns at which all 16 bits of the transmit data and the TCTL signal line are inverted. If any bit does not invert, this bit must be a skewed bit. Based on the data one clock cycle before and one clock cycle after this transition, the skewed bit can be corrected back. After the data skew is detected, a multiplexing logic circuitry is used to correct the skew based on one clock cycle either before or after the transition. The multiplexing logic circuitry includes at least three registers coupled to the inputs of the multiplexing logic circuitry.

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